265750 "3459580

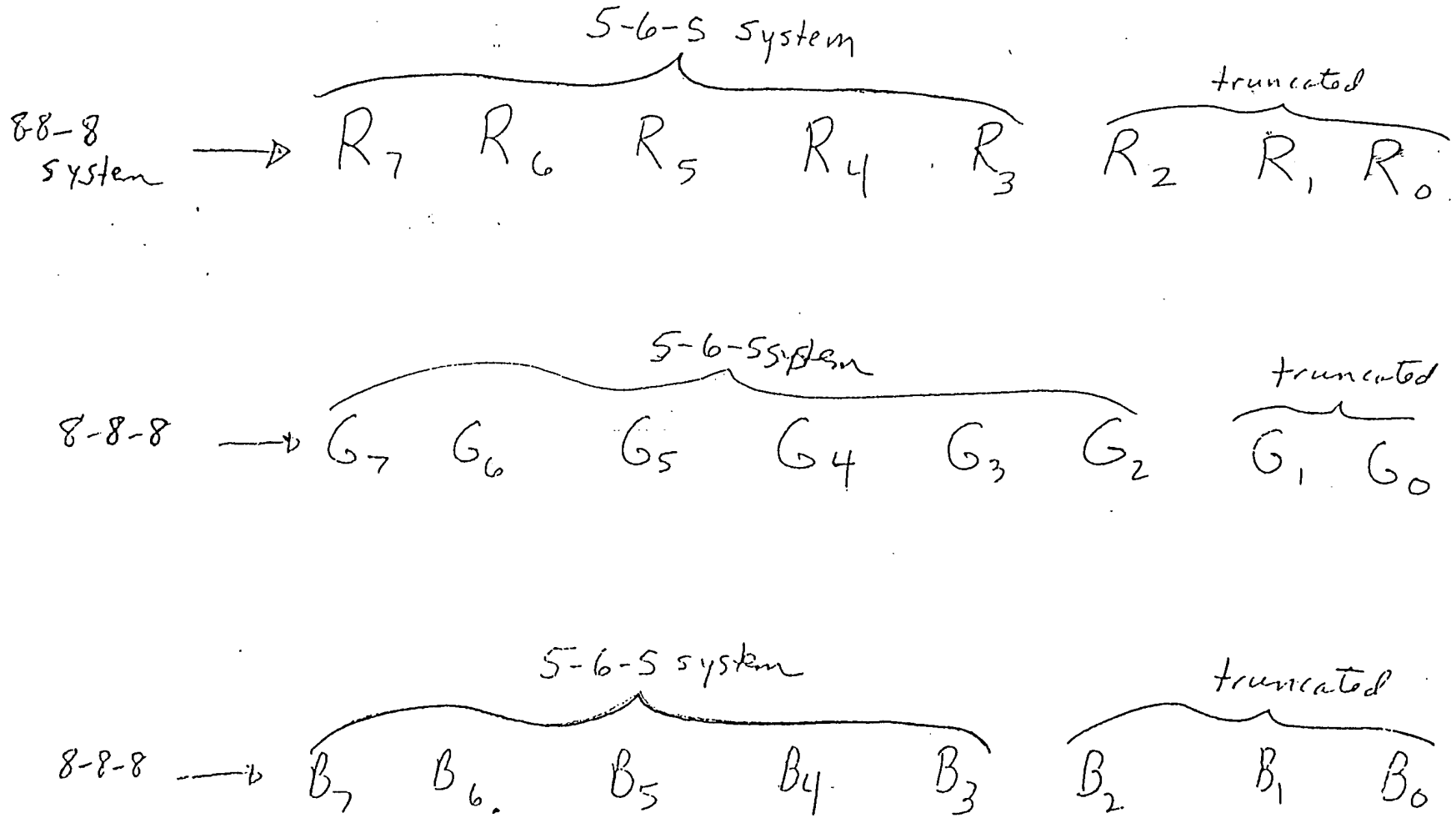

FIG. 1

		8 BIT								5 BIT				
		7	6	5	4	3	2	1	0	4	3	2	1	0
A		0	0	0	0	0	0	0	0	0	0	0	0	0
	1/8	0	0	0	0	0	0	0	1	0	0	0	0	0
	2/8	0	0	0	0	0	0	1	0	0	0	0	0	0
	3/8	0	0	0	0	0	0	1	1	0	0	0	0	0
	4/8	0	0	0	0	0	1	0	0	0	0	0	0	0
	5/8	0	0	0	0	0	1	0	1	0	0	0	0	0
	6/8	0	0	0	0	0	1	1	0	0	0	0	0	0
	7/8	0	0	0	0	0	1	1	1	0	0	0	0	0
A		0	0	0	0	1	0	0	0	0	0	0	0	1
	1/8	0	0	0	0	1	0	0	1	0	0	0	0	1
	2/8	0	0	0	0	1	0	1	0	0	0	0	0	1
	3/8	0	0	0	0	1	0	1	1	0	0	0	0	1
	4/8	0	0	0	0	1	1	0	0	0	0	0	0	1
	5/8	0	0	0	0	1	1	0	1	0	0	0	0	1
	6/8	0	0	0	0	1	1	1	0	0	0	0	0	1
	7/8	0	0	0	0	1	1	1	1	0	0	0	0	1
		0	0	0	1	0	0	0	0	0	0	0	1	0
	1/8	0	0	0	1	0	0	0	1	0	0	0	1	0
						.						.		
						.						.		
						.						.		

FIG. 2

Document: 6054954

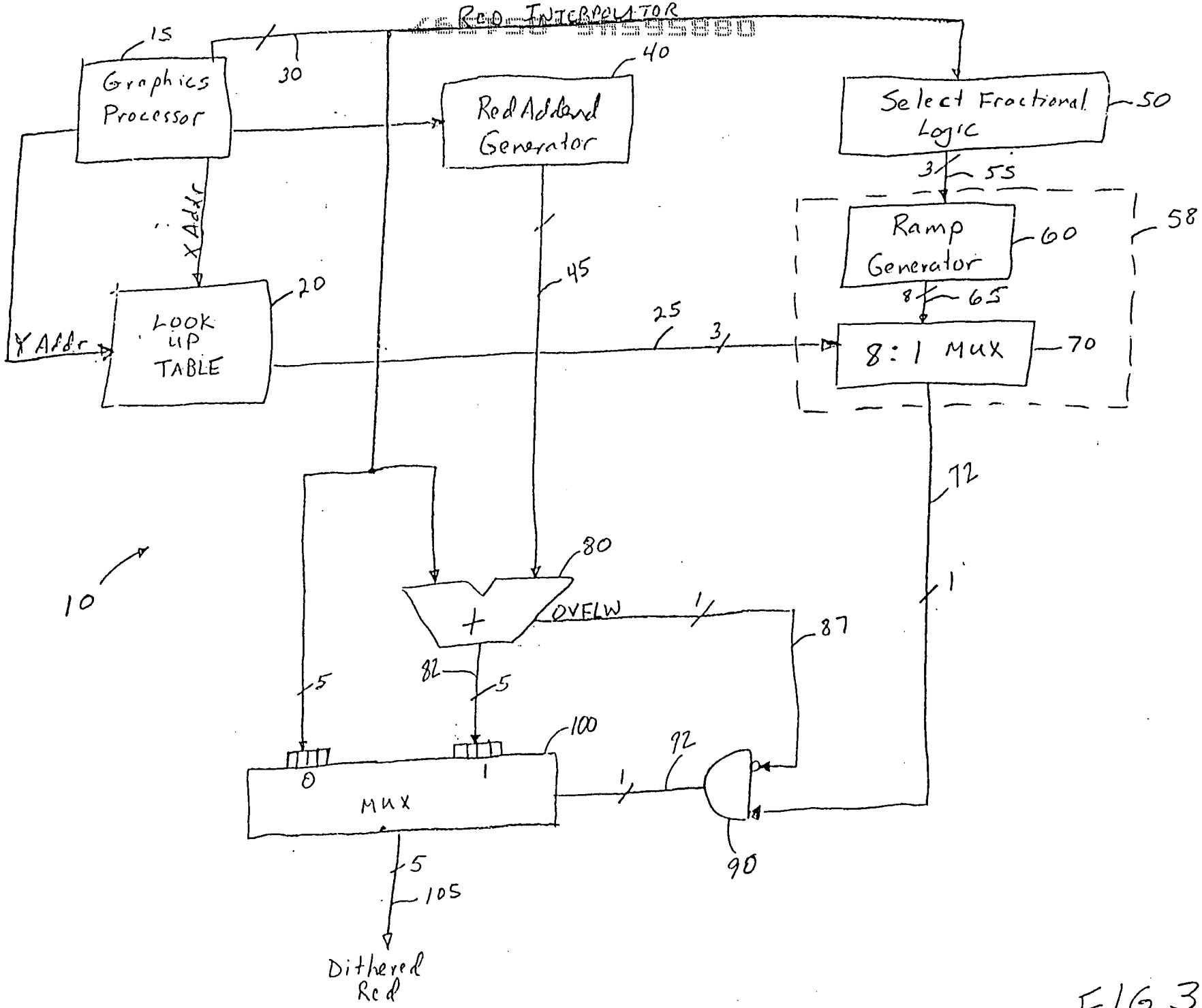
RGB INTERPOLATOR
15
Graphics Processor
30
40
Red Address Generator
Select Fractional Logic
50
3
55
Ramp Generator
60
58
8
65
X Addr
20
45
25
3
Y Addr
LOOK UP TABLE
8:1 MUX
70
72
10
80
+
OVFLW
1
87
82
5
5
100
0
1
MUX
1
72
90
5
105
Dithered Red

FIG. 3

20

Y Addr	X Addr 0	1	2	3	4	5	6	7
0	0	4	1	5	0	4	1	5
1	6	2	7	3	6	2	7	3
2	1	5	0	4	1	5	0	4
3	7	3	6	2	7	3	6	2
4	0	4	1	5	0	4	1	5
5	6	2	7	3	6	2	7	3
6	1	5	0	4	1	5	0	4
7	7	3	6	2	7	3	6	2

FIG. 4

Sheet 4 of 5

61

RAMP (5 bit system)

FRAC	Bit # 7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0
2	1	1	0	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	1	1	1	1	0	0	0	0
5	1	1	1	1	1	0	0	0
6	1	1	(1)	1	1	1	0	0
7	1	1	1	1	1	1	1	0

62

FIG. 5

64

RAMP (6 bit system)

FRAC	Bit # 3	2	1	0
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0

FIG. 6

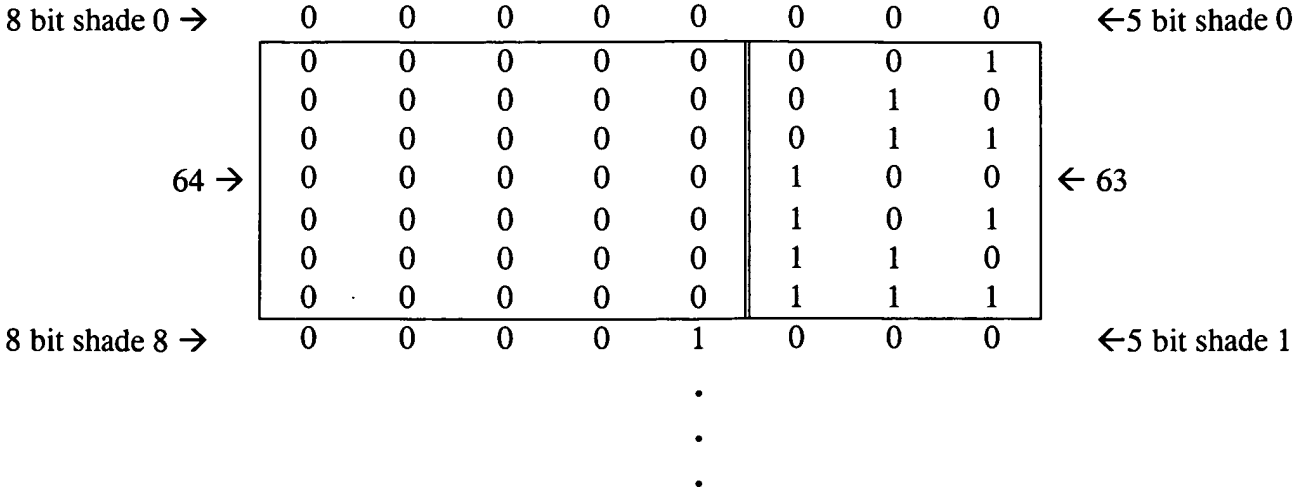
8 bit shade 0 →
0 0 0 0 0 0 0 0
←5 bit shade 0
0 0 0 0 0 0 0 1
0 0 0 0 0 0 1 0
0 0 0 0 0 0 1 1
64 →
0 0 0 0 0 1 0 0
← 63
0 0 0 0 0 1 0 1
0 0 0 0 0 1 1 0
0 0 0 0 0 1 1 1
8 bit shade 8 →
0 0 0 0 1 0 0 0
←5 bit shade 1

FIG. 7

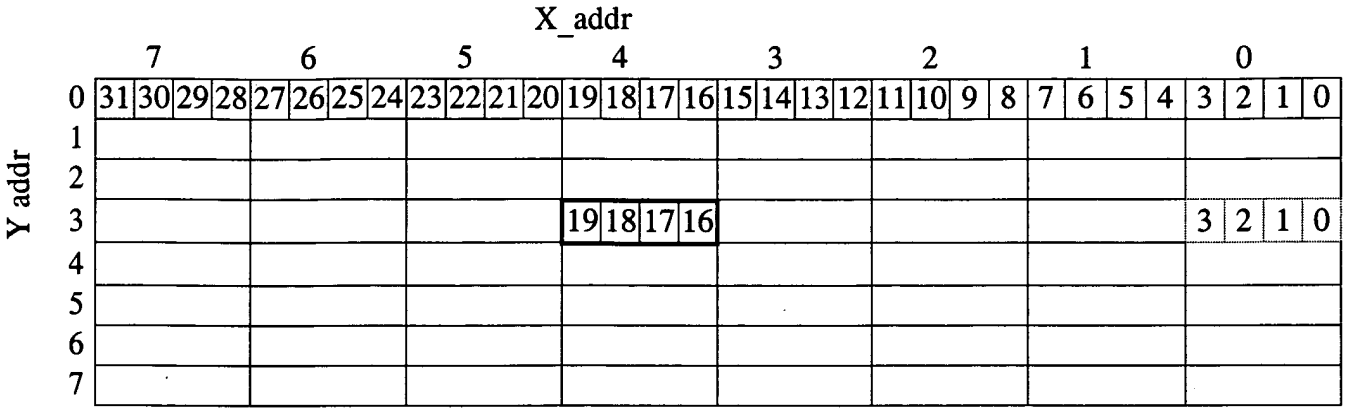
X_addr
7
6
5
4
3
2
1
0
Y addr
0 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1
2
3 19 18 17 16 3 2 1 0
4
5
6
7

FIG. 8